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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/645,789 | 08/20/2003 | Purna Mohanty | ADAPP243 | 8030 |

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| EXAMINER | |
|---|---|
| LIN, SUN J | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2825 | |

DATE MAILED: 01/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/645,789 | MOHANTY ET AL. | |
| | Examiner | Art Unit | |
| | Sun J Lin | 2825 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *20 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08/20/2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. This office action is in response to application 10/645,789 filed on 08/20/2003. Claims 1 – 20 remain pending in the application.

### *Specification Objections*

2. The specification is objected to because of following informalities:

Page 1, Paragraph 0001, update status of U.S. Patent Application entitled "***METHOD AND APPARATUS FOR ACCELERATING TEST CASE DEVELOPMENT***"

Appropriate correction is required.

### *Drawing Objections*

3. Drawings are objected to due to reasons listed in "***NOTICE OF DRAFTPERSON'S PATENT DRAWING REVIEW***" (PTO-948) attached with this office action. Appropriate correction is required.

### *Claim Objections*

4. Claims listed below are objected to because of the following informalities:

Claim 4, line 1, change "method operation" to **—method—**.
Claim 5, line 8, change "an" to **—the—**.
Claim 12, line 9, change "an" to **—the—**.

Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1 – 3, 5, 6, 10 – 12, 16 – 18 and 20 are rejected under 35 U.S.C. 102(b) as being unpatentable over U.S. Patent No. 6,324,671 B1 to *Ratzel et al.*

7. As to Claim 1, *Ratzel et al.* show and teach the following subject matter:

- A method for verifying *design goal* of an *integrated circuit design* – [col. 2, line 50 – 51];
- *Defining tasks*, the tasks being specified and formatted as text files using *high level design language* (HDL) such as *Verilog (HDL)* or *VHDL* – [col. 1, line 26 – 28; line 49 – 50]; Notice that the *Verilog* (HDL) is a *text based hardware description programming language*;
- *Specifying* (i.e., *Identifying*) a *timing test* (i.e., *test case*) – [Fig. 1A]; Notice that the *timing test* (*test case*) is defined by the *text based HDL tasks* – [Fig. 1A; col. 1, line 26 – 28; col. 8, line 40 – 67]; Notice that the *text based HDL tasks* are formatted as *text files*;
- *HDL text based tasks* are *behavioral description*, they need to be converted to *register-transfer level (RTL) description* for *verification* – [col. 1, line 26 – 33; col. 5, line 43 – 52]; Notice that *each of the tasks* is correlated with a *RTL description*;
- Process of *compiling an RTL description* to convert the *RTL description* into a list of *cells and interconnection* there between – [col. 1, line 63 – 66]; Notice that (1) a *compiled RTL description* is a *pre-compiled HDL task*; cells of *compiled RTL description* is stored in a *cell library* available for use in *synthesis tool* – col. 2, line 2 – 10] (2) *RTL modeling* and *synthesis tool* are applied for simulation;
- Executing the compiled task to simulate a behavior for the integrated circuit design to determine if timing goal has been achieved – [Step 12, 18, 22 and 24 in Fig. 1A];
- If *timing goal* has not been achieved, the tasks of the *timing test* (*test case*) are adjusted – [Step 26, 28 and 30 in Fig. 1A];
- Repeating the executing of the timing test (test case) to simulate the (timing) behavior for the integrated circuit design.

For reference purposes, the explanations given above in response to Claim 1 are called **[Response A]** hereinafter.

8. As to Claim 5, reasons are included in **[Response A]** given above. Notice that (1) the HDL tasks contain a sequence of tasks (2) a RTL behavioral model associated each HDL task need to be identified (3) simulation of the integrated circuited is performed using RTL modeling and synthesis tool – [Step 18, 20 and 22 in Fig. 1A] (4) pre-compiled HDL tasks are stored in cell library for future retrieval thereby minimizing compilation time.

For reference purposes, the explanations given above in response to Claim 5 are called **[Response B]** hereinafter.

9. As to Claim 12, reasons are included in **[Response B]** given above.

10. As to Claim 17, in addition to reasons included in **[Response A]** given above, *Ratzel et al.* show in Fig. 3 and teach a computer system for validating an integrated circuit design comprising (1) a processing unit 92 (i.e., processor) (2) a storage medium 96., which contains DRAM memory – [Fig. 3, col. 10, line 16 – col. 11, line 5]. Notice that (1) compiled tasks (i.e., RTL description) written in a HDL are stored in the storage medium 96 (2) a bus enabling communication between the processor, the memory and the storage medium.

11. As to Claims 2, 11 and 20, reasons are included in **[Response A]** given above.

12. As to Claim 3, there are many tasks need to be executed in verifying the goal of timing test. The tasks included in the timing test are grouped as macrotasks.

13. As to Claims 6 and 16, reasons are included in **[Response A]** given above. Notice that the HDL tasks are *precompiled* to achieve *compiled RTL description* being stored in cell library for retrieval.

14. As to Claim 10, *Ratzel et al.* show and teach storing the HDL tasks in a cell library of *pre-compiled HDL tasks* (*RTL description*) on storage device in communication

with a synthesis tool (i.e., system) performing the simulation – [Fig. 1A; Fig 2; col. 1, line 63 – col. 2, line 4]

15. As to Claim 18, *Ratzel et al.* teach that each step shown in Fig. 3 can be performed upon different computer systems. Furthermore, a *networked group* of *computer systems* may be used to perform the step shown in Fig. 3 – [Fig. 3; col. 11, line 1 – 5]. Since operating in a *networked group* of *computer systems*, the storage device can be externally located from a specific computer system.

***Claim Rejections - 35 USC § 103***

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

(1). Determining the scope and contents of the prior art.
(2). Ascertaining the differences between the prior art and the claims at issue.
(3). Resolving the level of ordinary skill in the pertinent art.
(4). Considering objective evidence present in the application indicating obviousness or nonobviousness.

17. Claims 4, 7, 9, 13, 15 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,324,671 B1 to *Ratzel et al.* in view of U.S. Patent No. 5,437,037 to *Furuichi.*

18. As to Claim 4, *Ratzel et al.* show and teach identifying a test case (timing test) defined by text based HDL tasks, they do not teach a method of verify a syntax and a format of each of the text based HDL tasks of the test case. But *Furuichi* teaches that the HDL file/program for use in simulation is created subjected to *syntax analysis* and *elements* (i.e., *tasks*) of the HDL file are decomposed according to *a predetermined*

*format* in order to redefine a database more suitable for processing a computer thereby the speed of execution of the simulation program is significantly improved – [col. 4, line 13 – 46].

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have applied the teachings of *Furuichi* in verifying syntax of the HDL file/program for use in simulation of timing test (test case) and verifying each of the *tasks* included in the HDL file to meet *a predetermined format* in order to redefine a database more suitable for processing a computer thereby the speed of execution of the simulation program is significantly improved.

For reference purposes, the explanations given above in response to Claim 4 are called **[Response C]** hereinafter.

19. As to Claims 7, 13 and 19, reasons are included in **[Response C]** given above.

20. As to Claim 9, *Ratzel et al.* show and teach identifying a test case (timing test) defined by text based HDL tasks; they do not teach a method of using program instructions for accessing a *translator layer* to correlate the tasks of the file with the (pre-compiled) HDL tasks. But *Furuichi* teaches using programming language descriptions (i.e., program instructions) for accessing the *translator 17*, such as *compiler and linker*, in association with a (cell) library in order to produce executable information 17a which can be executed by a computer 18 – [Fig. 4; col. 7, line 49 – 65]. Notice that function of the linker is to correlate the tasks of the file with pre-compiled HDL tasks (*compiled RTL description*), which are stored in the cell library.

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have applied the teachings of *Furuichi* in applying program instructions for accessing a *translator layer* to correlate the tasks of the file with the *pre-compiled HDL tasks (compiled RTL description)* already *stored in the cell library* in order to minimize compilation time thereby quickly producing executable information which can be executed by a computer.

For reference purposes, the explanations given above in response to Claim 9 are called **[Response CC]** hereinafter.

21. As to Claim 15, reasons are included in **[Response CC]** given above.

22. Claims 8 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,324,671 B1 to *Ratzel et al.* and U.S. Patent No. 5,437,037 to *Furuichi* in view of U.S. Patent No. 6,539,520 B1 to *Tiong et al.*

23. As to Claim 8, *Ratzel et al.* and *Furuichi* teach subject matter regarding verification of HDL of the file associated with the test case as recited in Claims 5 and 7, they do not teach a method of applying a *script* in performing the verification. But *Tiong et al.* teach utilizing *scripts* to eliminate the labor intensive processes of learning, memorizing syntax and debugging the HDL files to correct syntax errors – [col. 2, line 68 – col. 3, line 32].

Notice that the *script* provides a designer a useful and efficient way in verifying the HDL files associated with the test file, it eliminate the labor intensive processes of learning, memorizing syntax and debugging the HDL files to correct syntax errors.

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have applied the teachings of *Tiong et al.* in utilizing *scripts* in performing the verification of the file associated with the test case in order to eliminate the labor intensive processes of learning/memorizing syntax and debugging the HDL text files to correct syntax errors.

For reference purposes, the explanations given above in response to Claim 8 are called **[Response D]** hereinafter.

24. As to Claim 14, reasons are included in **[Response D]** given above.

***Conclusion***

25. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sun J Lin whose telephone number is (571) 272 - 1899. The examiner can normally be reached on Monday-Friday 9:30AM - 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on (571) 272 - 1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sun James Lin
Art Unit 2825
January 10, 2005